PENDING CLAIMS AND STATUS THEREOF

Claims 1-20 (canceled)

21. (new): A signal scaling circuit, comprising:

first, second and third capacitors connected to a first node;

a first switch connected between the first capacitor and a signal input;

a second switch connected between the first capacitor and a reference voltage;

a third switch connected between the second capacitor and the input signal;

a fourth switch connected between the second capacitor and the reference voltage;

a fifth switch connected between the third capacitor and the input signal;

a sixth switch connected between the third capacitor and the reference voltage;

a seventh switch connected in parallel with the first capacitor;

an eighth switch connected in parallel with the second capacitor;

a ninth switch connected in parallel with the third capacitor;

a tenth switch connected between a common mode voltage source and the first node;

an eleventh switch connected between the first node and an output of the signal scaling circuit; and

a switch controller for controlling the first through eleventh switches, wherein the switch controller controls opening and closing appropriate ones of the first through eleventh switches so that the output of the signal scaling circuit has a

second signal amplitude that is scaled to one-third or two-thirds of a first signal amplitude at the signal input.

22. (new): The signal scaling circuit according to claim 21, further comprising the switch controller shuffling the first, second and third capacitors for reducing error in the one-third or two-thirds amplitude scaling caused by any mismatch of capacitance values of the first, second and third capacitors.

23. (new): A signal scaling circuit, comprising:

M capacitors connected to a first node;

a plurality of first switches, each of the plurality of first switches being connected between a respective one of the M capacitors and a signal input;

a plurality of second switches, each of the plurality of second switches being connected between a respective one of the M capacitors and a reference voltage;

a plurality of third switches, each of the plurality of third switches being connected in parallel with a respective one of the M capacitors;

a fourth switch connected between the first node and a common mode voltage source; and

a switch controller, wherein the switch controller controls opening and closing the fourth switch and appropriate ones of the plurality of first, second and third switches so that the first node has a second signal whose amplitude is scaled by N/M of the amplitude of a first signal at the signal input, where N is less than M, and M and N are positive integer numbers.

24. (new): The signal scaling circuit according to claim 23, further comprising a fifth switch connected between the first node and an output of the signal scaling circuit, wherein the switch controller controls opening and closing of the fifth switch in combination with controlling the opening and closing of the fourth switch and the plurality of first, second and third switches.

25. (new): The signal scaling circuit according to claim 24, further comprising an operational amplifier having an input coupled to the output of the signal scaling circuit.

26. (new): The signal scaling circuit according to claim 25, wherein the operational amplifier is configured to be an inverting integrator.

27. (new): The signal scaling circuit according to claim 23, further comprising the switch controller shuffling the M capacitors for reducing error in the N/M scaling caused by any mismatch of capacitance values of the M capacitors.

28. (new): A differential signal scaling circuit, comprising:

M positive capacitors connected to a positive node;

a plurality of first positive switches, each of the plurality of first positive switches being connected between a respective one of the M positive capacitors and a positive signal input;

a plurality of second positive switches, each of the plurality of second positive switches being connected between a respective one of the M positive capacitors and a positive reference voltage;

a third switch connected between the positive node and a common mode voltage source;

M negative capacitors connected to a negative node;

a plurality of first negative switches, each of the plurality of first negative switches being connected between a respective one of the M negative capacitors and a negative signal input;

a plurality of second negative switches, each of the plurality of second negative switches being connected between a respective one of the M negative capacitors and a negative reference voltage;

a fourth switch connected between the negative node and a common mode voltage source;

a plurality of fifth switches, each of the plurality of fifth switches being connected between respective ones of the M positive and M negative capacitors;

a sixth switch connected between the positive and negative nodes; and

a switch controller, wherein the switch controller controls opening and closing the third, fourth and sixth switches, appropriate ones of the plurality of first and second positive and negative switches, and appropriate ones of the plurality of fifth switches so that the positive node has a second positive signal that is N/M the amplitude of a first positive signal at the positive signal input and the negative node has a second negative signal that is N/M the amplitude of a first negative signal at the negative signal input, where N is less than M, and M and N are positive integer numbers.

29. (new): The differential signal scaling circuit according to claim 28, further comprising seventh positive and negative switches connected between the positive and negative nodes and positive and negative outputs, respectively, of the signal scaling circuit,

wherein the switch controller controls opening and closing of the seventh positive and negative switches in combination with controlling the opening and closing of the third, fourth and sixth switches, appropriate ones of the plurality of first and second positive and negative switches, and appropriate ones of the plurality of fifth switches.

30. (new): The differential signal scaling circuit according to claim 29, further comprising a differential operational amplifier having positive and negative inputs coupled to the positive and negative outputs of the signal scaling circuit.

31. (new): The differential signal scaling circuit according to claim 30, wherein the differential operational amplifier is configured to be an inverting integrator.

32. (new): The differential signal scaling circuit according to 28, further comprising the switch controller shuffling the M positive capacitors and shuffling the M negative capacitors for reducing error in the N/M scaling caused by any mismatch of capacitance values of the M positive capacitors, and any mismatch of capacitance values of the M negative capacitors.